REMARKS AND ARGUMENTS

Status of the Application

Claims 2, 3, 6-7, 9-23 and 25-33 are pending in the subject application. Claims 2-3, 6-7, 9-16 and 25-33 are rejected under 35 USC § 102(e). Claims 17-23 are objected as being dependent upon a rejected base claim. By way of this amendment, Applicant has amended claims 2, 6, 15, 16-18 and 25-26 and added new claims 34 and 35.

Rejection under 35 USC §102

Claims 2-3, 6-7, 9-16 and 25-33 are rejected under 35 USC §102(e) as being anticipated by Wang et al. (Pub US Patent No. 2002/0194558). Applicant respectfully disagrees.

Claim 2, as amended, recites a memory array having a plurality of banks. Each bank is associated with a comparator unit. A BIST control unit is coupled to the memory array. The BIST generates control signals and a test pattern for testing the memory array. By associating one comparator unit with each memory bank, the plurality of memory banks can be tested simultaneously by having each comparator unit compare a word read from its associated memory bank with the test pattern written. Claims 15 and 25, like claim 2, recite a plurality of comparator units, each associated with a memory bank to facilitate testing of the plurality of memory banks simultaneously except that in claim 15, the memory cells are dual port memory cells while in claim 25, at least one comparator is associated with each memory bank.

Wang et al. describes a BIST controller for testing one or more memory arrays. In contrast to the presently claimed invention, Wang et al. provides only one comparator in the BIST controller. *See* Wang et al., paragraph [0080], claim 6 and Fig. 1 (element 107). Since

only one comparator is associated with the whole array, each bank of the array cannot be associated with its own comparator, as presently claimed. Furthermore, this would result in only one word from the whole array being tested at any one time. As such, it would be impossible to test all the banks of the array simultaneously, as suggested by the Examiner. Providing one or at least one comparator to each bank of an array to facilitate simultaneous testing of the plurality of banks is nowhere taught or suggested by Wang et al. Therefore, Applicant submits that claims 2, 15 and 25 are patentable over Wang et al. Since claims 3, 6-7, 9-14, 16, 26-33 and new claims 34-35 are directly or indirectly dependent on claims 2, 15, and 25, these claims are also patentable.

Allowable Subject Matter

Claims 17-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all the limitations of the base claim and any intervening claims. In response, Applicant has amended claim 17 to be in independent form, including all of the limitations of the base claim and any intervening claims. Applicant submits that claim 17 is now patentable over the cited art of record and respectfully requests the withdrawal of the objection. Since claims 18-23 are directly or indirectly dependent on claim 17, these claims are also patentable.

Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

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Respectfully submitted,

Dexter Chin
Attorney for Applicant
Reg. No. 38,842

Horizon IP Pte Ltd
166 Kallang Way, 6th Floor
Singapore 349249
Tel.: (65) 9836 9908
Fax: (65) 6746 8263